X-Ray Inspection and its Effect on NAND Flash Memory

Executive Summary

Production bottlenecks and high cost of programming large files at test make preprogramming the preferred method for production managers building product using high-density eMMC NAND flash. While there are several well documented papers to validate that X-Ray inspection can impact data retention in preprogrammed eMMC NAND devices, little is mentioned regarding technology advancements designed to correct eMMC data retention errors including bit-flips. This paper is intended to help production managers better understand eMMC NAND with a focus on the technology safeguards and recommended best practices to ensure data integrity from the time the eMMC device is preprogrammed to final product. Error correction code (ECC) enabled eMMC devices preserve data integrity and are essentially immune to "reasonable" doses of irradiation.

Semiconductor vendors are continuously enhancing the error correction capabilities for eMMC NAND flash. In fact, Cypress Semiconductor recently commented;

"Error correction code (ECC) protected eMMC are soft error immune until accumulated multiple bit upset (MBU) events occur. The probability of those events are **thousands of years** in real life environments and only need to be carefully taken into account during accelerated beam testing.

*Source: Cypress Semiconductor Reliability Report, Document No. 002-11604 Rev: ***

eMMC NAND features Error Correction Code (ECC) Software

eMMC NAND consists of RAW NAND flash memory and a controller to manage bit errors. By detecting and correcting single-bit errors, ECC helps preserve integrity of the data, prevents data corruption and prevents system crashes and failures. The diagram below shows the progression of NAND bit flips from release through X-Ray inspection. ECC corrects data as a result of error bits resident in NAND, preserving the data integrity used by the final product.

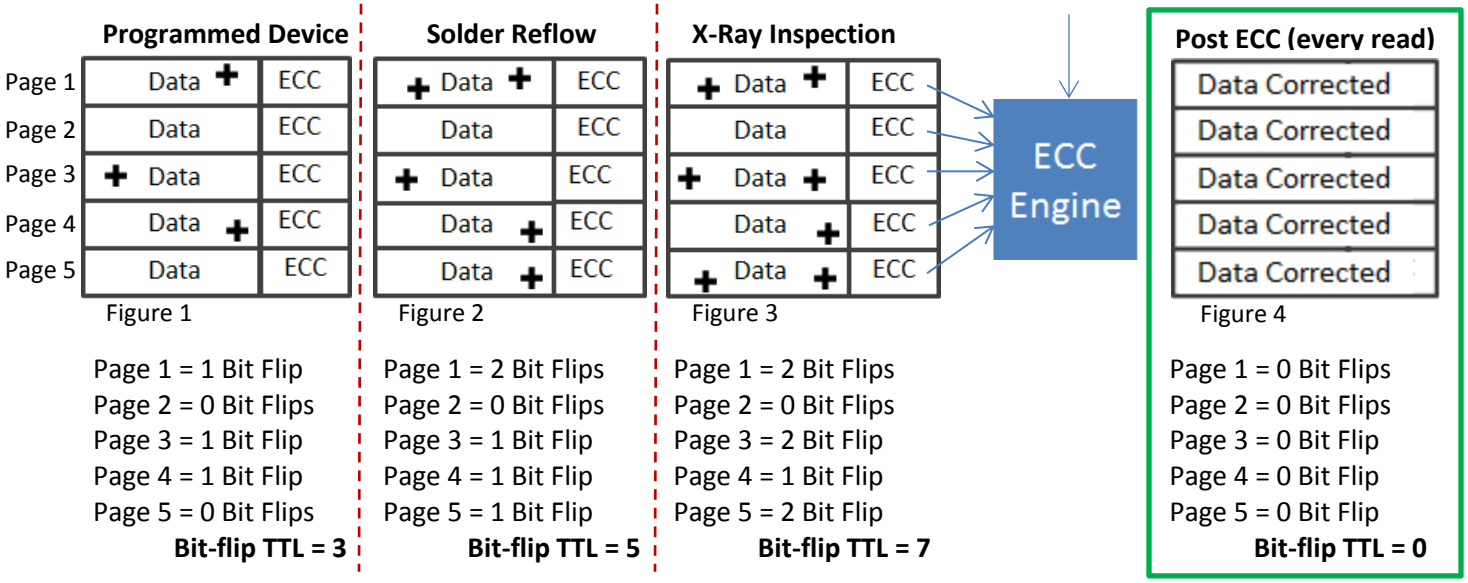
Figure 1: factory device shipped with 3 bit errors. Successfully Programmed

Figure 2: at solder reflow, 2 addition bit errors occur, for a total of 5

Figure 3: at X-Ray inspection, 2 additional bit errors occur, for a total of 7

Note: after years of usage (continuous Read Access), a few additional bit errors may occur and get corrected by ECC

Figure 4: every time the data is read from memory, the ECC Engine will correct any bit errors and present the corrected data to the processor/application



Addition Safeguards to Mitigate Bit Flips at X-Ray Inspection

The following are the some recommended mitigation techniques to minimize the effects of any potential data retention issues resulting from X-ray inspection. As there are many commercially available circuit board inspection systems with different setup conditions and exposure doses, it is not possible to provide a single set of recommendations that will apply to all inspection systems.

- Use a 300-µm thick Zn filter; 1-mm thick Al or Brass filters.
- Use the smallest X-ray tube kV-peak possible that still produces adequate images during board inspection.
- Use the smallest X-ray tube current possible that produces adequate images.
- Use the largest X-ray tube to sample distance (i.e. lowest magnification) possible.
- Use the shortest inspection time possible, preferably on a sampling basis rather than 100% board inspection.
- If X-ray inspection is performed after the flash has been programmed, consider booting the final product and performing a block refresh (erase and reprogram).

Sources: Spansion - Xray_Inspection_Test_Conditions_AN, Rev 01
Intersil Application Note: 1533

A leading NAND supplier recommends operating the X-ray dose to NAND at less ≤1 Gy

- 1Gy = 100 rads (units of irradiation)
- *1Gy of X-rays is an order of magnitude greater than 0.1Gy specified in ISO7816-1*

Source: Leading NAND Supplier

Summary

All NAND flash architectures suffer from a phenomenon known as “bit-flipping”. On some occasions including natural wear, at solder reflow and/or X-Ray inspection a bit or bits are either flipped, or is reported flipped. To correct bit-flips an error correction code (ECC) algorithm must be applied.

Today’s ECC-enabled eMMC devices are essentially immune to what one would consider “reasonable” doses of irradiation. Consider that eMMC NAND having 42-bit Error Correction Code (ECC) is not likely to produce an error in 1000 years of operation.

Preprogramming is fine for today’s eMMC devices when processed through X-Ray inspection while following best practices. For confirmation, it’s always recommended to perform a trial run and confirm the test results yourself.